Design Review #2

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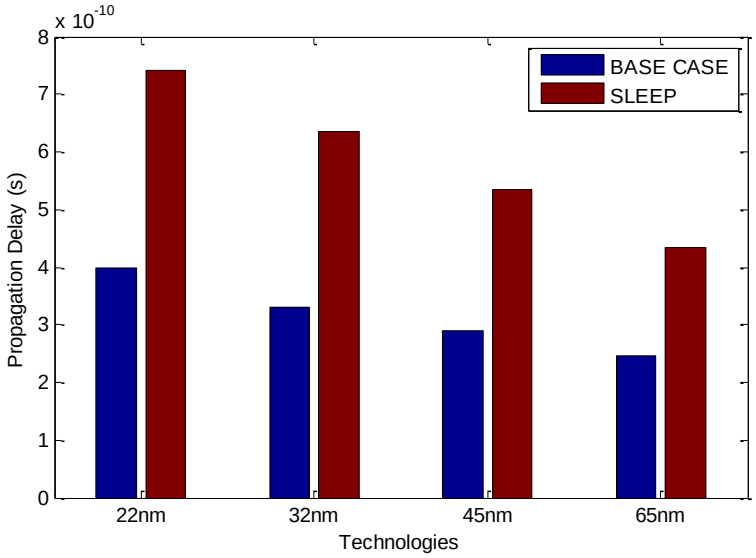
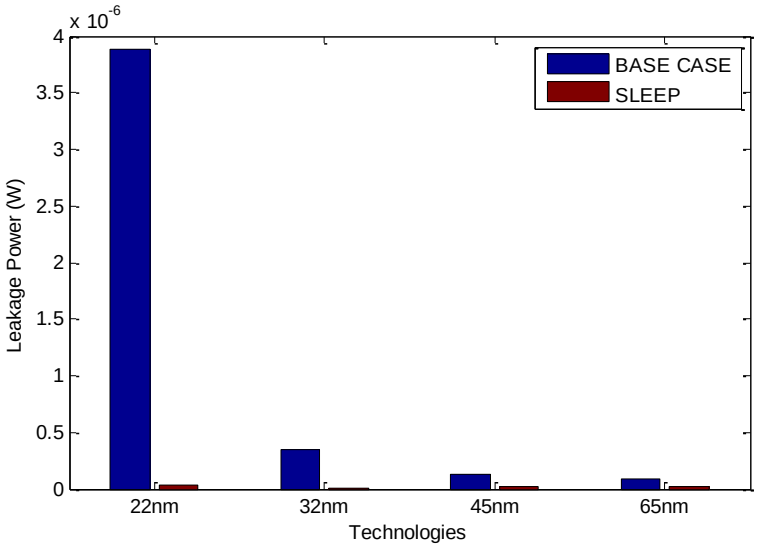
* Projects Progress

First Step (Nov. 2nd Week)

- Target Netlist: BASE CASE, SLEEP CASE
- Simulation : Cadence Ocean Transient Simulation
- What is supposed to be showed : Delay, Leakage Power
- Variation of parameters : Technologies(22nm, 32nm, 45nm, 65nm),



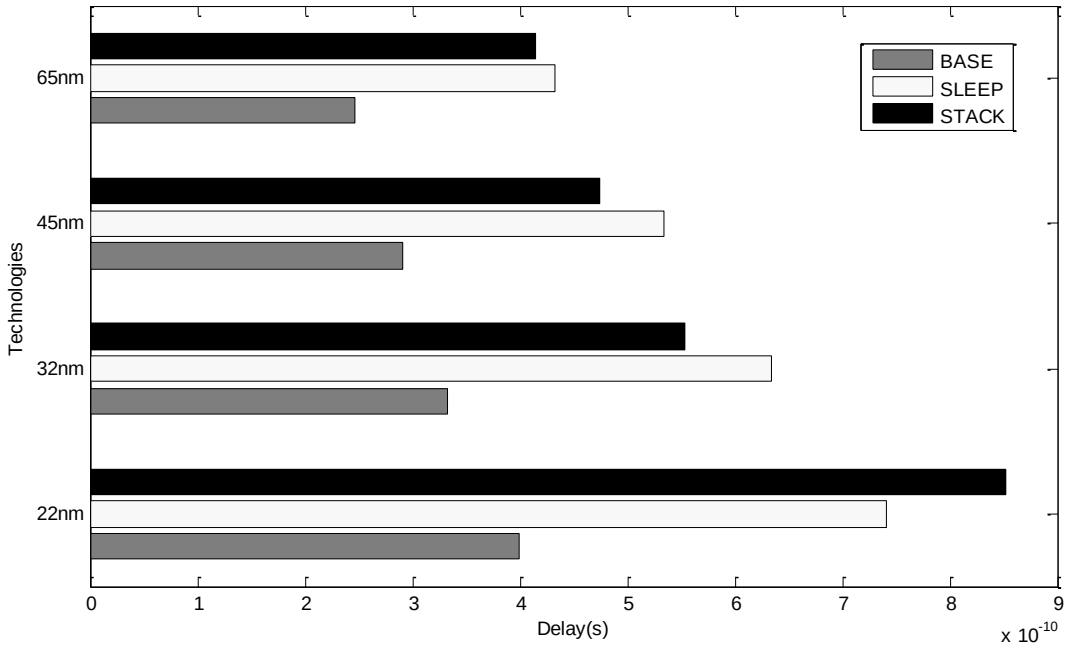


Random Circuit	Propagation Delay(s)	Leakage Power(W)
Base Case(22nm)	3.997373e-10	3.881886e-06
Base Case(32nm)	3.319460e-10	3.456075e-07
Base Case(45nm)	2.906834e-10	1.234292e-07
Base Case(65nm)	2.461198e-10	8.404825e-08
Sleep(22nm)	7.413818e-10	3.072531e-08
Sleep(32nm)	6.346789e-10	1.193364e-08
Sleep(45nm)	5.340086e-10	1.421527e-08
Sleep(65nm)	4.327406e-10	2.212812e-08

Second Step (Nov. 3nd Week)

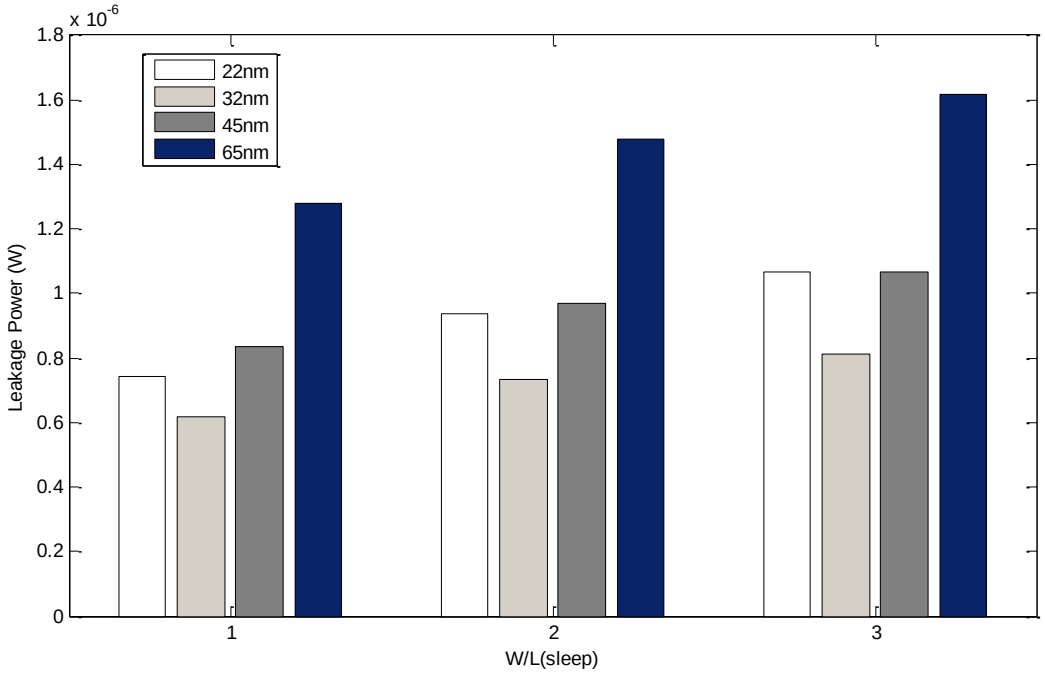
- Target Netlist: BASE CASE, SLEEP CASE, STACK CASE, (BodyBias?)
- Simulation: Statistical Monte Carlo 50 repetitions
- What is supposed to be showed: Delay, Eact, Elk/Ilk
- Variation of parameters: Technologies (22nm, 32nm, 45nm, 65nm), Width(W), Sharing sleep or stack Transistor.

- Delay Analysis (3 Technique, 4 Technologies)



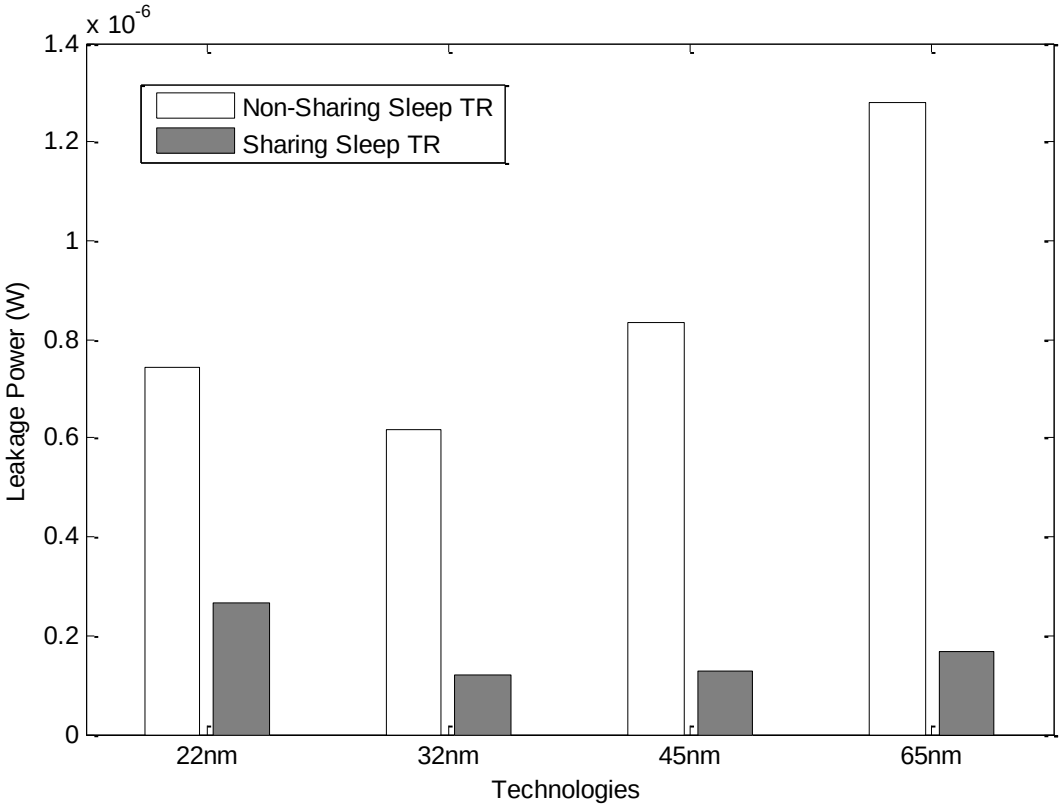
Technologies	Propagation Delay(s)		
	BASE	SLEEP	STACK
22nm	3.997373e-10	7.413818e-10	8.514665e-10
32nm	3.319460e-10	6.346789e-10	5.534887e-10
45nm	2.906834e-10	5.340086e-10	4.738065e-10
65nm	2.461198e-10	4.327406e-10	4.147967e-10

- Leakage vs Width (Sleep Technique, 4 Technologies)



Technologies	Leakage		
	W/L(sleep) = 2	W/L(sleep) = 4	W/L(sleep) =6
22nm	7.420567e-07	9.363757e-07	1.065078e-06
32nm	6.155349e-07	7.324606e-07	8.131706e-07
45nm	8.340274e-07	9.710812e-07	1.066361e-06
65nm	1.281556e-06	1.479970e-06	1.618668e-06

- Leakage vs Sharing Sleep



Technologies	Non-Sharing Sleep TR	Sharing Sleep TR
22nm	7.420567e-07	2.657642e-07
32nm	6.155349e-07	1.213040e-07
45nm	8.340274e-07	1.263703e-07
65nm	1.281556e-06	1.691219e-07

- Leakage Analysis (3 Technique, 4 Technologies)

- Leakage Power Analysis (3 Technique, 4 Technologies)

- Active Power Analysis (3 Technique, 4 Technologies)

Appendix (Netlists)

1. Base Case Netlist

```
// Written by Taeyoung
// Input and Source
VVDD ( VDD 0 ) vsource dc=pvdd
VVSS ( VSS 0 ) vsource dc=0
VVIN ( A 0 ) vsource type=pulse val0=0 val1=pvdd delay=5n width=5n period=10n
rise=0.01n fall=0.01n
//VVIN ( A 0 ) vsource dc=pvdd

// subckt NETLIST
// TK

subckt TKInv VDD VSS in out
    MP1 (out in VDD VDD) PFET w=wdef l=ldef
    MN1 (out in VSS VSS) NFET w=wdef l=ldef
ends TKInv

subckt TKNand VDD VSS inA inB out
    MP1 (out inA VDD VDD) PFET w=wdef l=ldef
    MP2 (out inB VDD VDD) PFET w=wdef l=ldef
    MN1 (out inA X1 VSS) NFET w=wdef l=ldef
    MN2 (X1 inB VSS VSS) NFET w=wdef l=ldef
ends TKNand

subckt TKNor VDD VSS inA inB out
    MP1 (X1 inA VDD VDD) PFET w=wdef l=ldef
    MP2 (out inB X1 VDD) PFET w=wdef l=ldef
    MN1 (out inA VSS VSS) NFET w=wdef l=ldef
    MN2 (out inB VSS VSS) NFET w=wdef l=ldef
ends TKNor

// CKT which has 3 path

// path 1
INV1_1 ( VDD VSS A A1_1 ) TKInv
INV1_2 ( VDD VSS A1_1 A1_2 ) TKInv
INV1_3 ( VDD VSS A1_2 A1_3 ) TKInv
INV1_4 ( VDD VSS A1_3 A1_4 ) TKInv
INV1_5 ( VDD VSS A1_4 A1_5 ) TKInv
INV1_6 ( VDD VSS A1_5 A1_6 ) TKInv
INV1_7 ( VDD VSS A1_6 AOUT ) TKInv


// path 2
INV2_1 ( VDD VSS A A2_1 ) TKInv
INV2_2 ( VDD VSS A2_1 A2_2 ) TKInv
INV2_3 ( VDD VSS A2_2 A2_3 ) TKInv
NAND2_1 ( VDD VSS A2_3 A1_3 A2_4 ) TKNand
INV2_4 ( VDD VSS A2_4 A2_5 ) TKInv
INV2_5 ( VDD VSS A2_5 BOUT ) TKInv

// path 3
INV3_1 ( VDD VSS A A3_1 ) TKInv
INV3_2 ( VDD VSS A3_1 A3_2 ) TKInv
NOR3_1 ( VDD VSS A3_2 A2_2 A3_3 ) TKNor
INV3_3 ( VDD VSS A3_3 COUT ) TKInv

// Fianl
NAND4_1 (VDD VSS AOUT BOUT FOUT ) TKNand
NAND4_2 (VDD VSS FOUT COUT GOUT ) TKNand
```

```
// Load
c1 (GOUT 0) capacitor c=20f
```

2. Base Case with Sleep TR NETLIST

```
// Written by Taeyoung

// Input and Source
VVDD ( VDD 0 ) vsource dc=pvdd
VVSS ( VSS 0 ) vsource dc=0
VVIN ( A 0 ) vsource type=pulse val0=0 val1=pvdd delay=5n width=5n period=10n
rise=0.01n fall=0.01n
//VVIN ( A 0 ) vsource dc=pvdd
// Sleep signal controlled by OCN script don't touch here.
VVSL ( SL 0 ) vsource dc=svdd

// subckt NETLIST
// TK

subckt TKInv VDD VSS in out sleep
    MP1 (out in VDD VDD) PFET w=wdef l=ldef
    MN1 (out in slVSS slVSS) NFET w=wdef l=ldef
    MNSLEEP (slVSS sleepb VSS VSS) NFET w=wdef l=ldef
ends TKInv

subckt TKNand VDD VSS inA inB out sleep
    MP1 (out inA VDD VDD) PFET w=wdef l=ldef
    MP2 (out inB VDD VDD) PFET w=wdef l=ldef
    MN1 (out inA X1 VSS) NFET w=wdef l=ldef
    MN2 (X1 inB slVSS slVSS) NFET w=wdef l=ldef
    MNSLEEP (slVSS sleepb VSS VSS) NFET w=wdef l=ldef
ends TKNand

subckt TKNor VDD VSS inA inB out sleep
    MP1 (X1 inA VDD VDD) PFET w=wdef l=ldef
    MP2 (out inB X1 VDD) PFET w=wdef l=ldef
    MN1 (out inA slVSS slVSS) NFET w=wdef l=ldef
    MN2 (out inB slVSS slVSS) NFET w=wdef l=ldef
    MNSLEEP (slVSS sleepb VSS VSS) NFET w=wdef l=ldef
ends TKNor

// CKT which has 3 path

// path 1
INV1_1 ( VDD VSS A A1_1 SL ) TKInv
INV1_2 ( VDD VSS A1_1 A1_2 SL ) TKInv
INV1_3 ( VDD VSS A1_2 A1_3 SL ) TKInv
INV1_4 ( VDD VSS A1_3 A1_4 SL ) TKInv
INV1_5 ( VDD VSS A1_4 A1_5 SL ) TKInv
INV1_6 ( VDD VSS A1_5 A1_6 SL ) TKInv
INV1_7 ( VDD VSS A1_6 AOUT SL ) TKInv


// path 2
INV2_1 ( VDD VSS A A2_1 SL ) TKInv
INV2_2 ( VDD VSS A2_1 A2_2 SL ) TKInv
INV2_3 ( VDD VSS A2_2 A2_3 SL ) TKInv
NAND2_1 ( VDD VSS A2_3 A1_3 A2_4 SL ) TKNand
INV2_4 ( VDD VSS A2_4 A2_5 SL ) TKInv
INV2_5 ( VDD VSS A2_5 BOUT SL ) TKInv
```

```
// path 3
INV3_1 ( VDD VSS A A3_1 SL ) TKInv
INV3_2 ( VDD VSS A3_1 A3_2 SL ) TKInv
NOR3_1 ( VDD VSS A3_2 A2_2 A3_3 SL ) TKNor
INV3_3 ( VDD VSS A3_3 COUT SL ) TKInv

// Fianl
NAND4_1 (VDD VSS AOUT BOUT FOUT SL ) TKNand
NAND4_2 (VDD VSS FOUT COUT GOUT SL ) TKNand

// Load
c1 (GOUT 0) capacitor c=20f
```

3. Base Case with Stack TR Netlist

```
// Written by Taeyoung

// Input and Source
VVDD ( VDD 0 ) vsource dc=pvdd
VVSS ( VSS 0 ) vsource dc=0
VVIN ( A 0 ) vsource type=pulse val0=0 val1=pvdd delay=5n width=5n period=10n
rise=0.01n fall=0.01n
//VVIN ( A 0 ) vsource dc=pvdd

// subckt NETLIST
// TK

subckt TKInv VDD VSS in out
    MPSTACK (X1 in VDD VDD) PFET w=wdef l=ldef
    MP1 (out in X1 VDD) PFET w=wdef l=ldef
    MN1 (out in X2 VSS) NFET w=wdef l=ldef
    MNSTACK (X2 in VSS VSS) NFET w=wdef l=ldef
ends TKInv

subckt TKNand VDD VSS inA inB out
    MP1STACK (stVDD1 inA VDD VDD) PFET w=wdef l=ldef
    MP2STACK (stVDD2 inB VDD VDD) PFET w=wdef l=ldef
    MP1 (out inA stVDD1 VDD) PFET w=wdef l=ldef
    MP2 (out inB stVDD2 VDD) PFET w=wdef l=ldef
    MN1 (out inA X1 VSS) NFET w=wdef l=ldef
    MN2 (X1 inB stVSS1 VSS) NFET w=wdef l=ldef
    MN1STACK (stVSS1 inA stVSS2 VSS) NFET w=wdef l=ldef
    MN2STACK (stVSS2 inB VSS VSS) NFET w=wdef l=ldef
ends TKNand

subckt TKNor VDD VSS inA inB out
    MP1STACK (stVDD1 inA VDD VDD) PFET w=wdef l=ldef
    MP2STACK (stVDD2 inB stVDD1 VDD) PFET w=wdef l=ldef
    MP1 (X1 inA stVDD2 VDD) PFET w=wdef l=ldef
    MP2 (out inB X1 VDD) PFET w=wdef l=ldef
    MN1 (out inA stVSS1 VSS) NFET w=wdef l=ldef
    MN2 (out inB stVSS2 VSS) NFET w=wdef l=ldef
    MN1STACK (stVSS1 inA VSS VSS) NFET w=wdef l=ldef
    MN2STACK (stVSS2 inB VSS VSS) NFET w=wdef l=ldef
ends TKNor

// CKT which has 3 path

// path 1
INV1_1 ( VDD VSS A A1_1 ) TKInv
```

```
INV1_2 ( VDD VSS A1_1 A1_2 ) TKInv
INV1_3 ( VDD VSS A1_2 A1_3 ) TKInv
INV1_4 ( VDD VSS A1_3 A1_4 ) TKInv
INV1_5 ( VDD VSS A1_4 A1_5 ) TKInv
INV1_6 ( VDD VSS A1_5 A1_6 ) TKInv
INV1_7 ( VDD VSS A1_6 AOUT ) TKInv


// path 2
INV2_1 ( VDD VSS A A2_1 ) TKInv
INV2_2 ( VDD VSS A2_1 A2_2 ) TKInv
INV2_3 ( VDD VSS A2_2 A2_3 ) TKInv
NAND2_1 ( VDD VSS A2_3 A1_3 A2_4 ) TKNand
INV2_4 ( VDD VSS A2_4 A2_5 ) TKInv
INV2_5 ( VDD VSS A2_5 BOUT ) TKInv

// path 3
INV3_1 ( VDD VSS A A3_1 ) TKInv
INV3_2 ( VDD VSS A3_1 A3_2 ) TKInv
NOR3_1 ( VDD VSS A3_2 A2_2 A3_3 ) TKNor
INV3_3 ( VDD VSS A3_3 COUT ) TKInv

// Fianl
NAND4_1 (VDD VSS AOUT BOUT FOUT ) TKNand
NAND4_2 (VDD VSS FOUT COUT GOUT ) TKNand

// Load
c1 (GOUT 0) capacitor c=20f
```